R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, in FIGS. 1 and 2 and in the specification as originally filed, for example, on page 5, line 18 through page 8, line 6 and on page 19, line 18 through page 20, line 13. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1-4, 8, 9 and 20 under 35 U.S.C. §102(e) as being anticipated by Sexton (U.S. Patent No. 6,769,116) has been obviated by amendment and should be withdrawn.

In contrast to Sexton, the presently claimed invention (claim 1) provides an apparatus comprising an analysis block, a graphic user interface and a memory circuit. The analysis block may be configured to generate debug information post-simulation in response to (i) a command input, (ii) one or more simulation outputs, (iii) one or more compiler outputs and (iv) memory map information. The graphical user interface may be configured (i) to present the command input in response to one or more user input parameters and (ii) to display the debug information. The memory

circuit may be configured to store the memory map information, the one or more simulation outputs and the one or more compiler outputs. The one or more simulation outputs comprise one or more tracings selected from the group consisting of a tracing of processor accesses on a memory bus, a tracing of instruction execution and a tracing of processor internal register status. The one or more compiler outputs comprise one or more outputs selected from the group consisting of a map file and an in-line disassembler. Claims 10 and 20 include similar limitations. Sexton does not disclose or suggest generating debug information post-simulation, as presently claimed. Specifically, Sexton uses breakpoints triggered during simulation to detect operations that cause memory corruption (Abstract of Sexton). As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-4, 8 and 9 depend, directly or indirectly, from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claim 5 under 35 U.S.C. §103 as being unpatentable over Sexton (U.S. Patent No. 6,769,116) in further

view of Pauna (U.S. Patent No. 6,052,524) has been obviated by amendment and should be withdrawn.

The rejection of claims 6 and 7 under 35 U.S.C. §103(a) as being unpatentable over Sexton in further view of Examiner's Official Notice of "frames" and "windows" has been obviated by amendment and should be withdrawn.

The rejection of claims 10, 12, and 14-19 under 35 U.S.C. §103(a) as being unpatentable over Sexton in view of Pauna has been obviated by amendment and should be withdrawn.

The rejection of claims 11 and 13 under 35 U.S.C. §103(a) as being unpatentable over Sexton in view of Pauna and further in view of Examiner's Official Notice of "assembly code" has been obviated by amendment and should be withdrawn.

In contrast to the cited references, the presently claimed invention (claim 1) provides an apparatus comprising an analysis block, a graphic user interface and a memory circuit. The analysis block may be configured to generate debug information post-simulation in response to (i) a command input, (ii) one or more simulation outputs, (iii) one or more compiler outputs and (iv) memory map information. The graphical user interface may be configured (i) to present the command input in response to one or more user input parameters and (ii) to display the debug information. The memory circuit may be configured to store the memory map information, the one or more simulation outputs and the

one or more compiler outputs. The one or more simulation outputs comprise one or more tracings selected from the group consisting of a tracing of processor accesses on a memory bus, a tracing of instruction execution and a tracing of processor internal register status. The one or more compiler outputs comprise one or more outputs selected from the group consisting of a map file and an in-line disassembler. Claim 10 includes similar limitations. The cited references do not appear to disclose or suggest generating debug information post-simulation, as presently claimed. Specifically, the cited references all use breakpoints for interactive debugging during simulation. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Furthermore, with respect to the rejection of claims 11 and 13 based upon the Examiner taking Official Notice that "assembly code" is well known, the statement in the Office Action that "[a] person of ordinary skill in the art at the time of the invention would have been motivated to use assembly because it is faster than programming in machine code and provides efficient control over processor operations" does not appear to address the use of assembler instruction codes as debug information, as presently claimed. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

New claims 21 and 22 depend directly from claim 1, which is believed to be allowable. Furthermore, the cited references do not teach or suggest post-processing simulation results or generating debug information without interacting with a processor simulator or processor simulation model. As such, the presently claimed invention is fully patentable over the cited references.

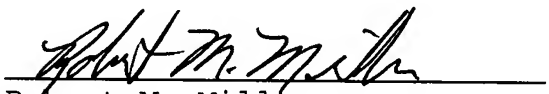
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative between the hours of 9 a.m. and 5 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892

Dated: August 29, 2007

c/o David Smith
LSI Corporation

Docket No.: 03-1868 / 1496.00348